Remarks

Applicant has cancelled claims 1 and 2. Claims 5-7, 9-11, 19 and 28 are currently amended. Claims 8, 13, 15-18, 23-27, 29 and 30 remain currently unchanged.

Applicant hereby requests further examination since applicant believes the amended claims and the claims remaining unchanged place the application in a condition for allowance.

IN THE CLAIMS

I. Claim rejections under 35 USC §112

The Examiner rejected claims 19 and 23-30 "under U.S.C. 112, second paragraph, as being indefinite for failing to particularly point and distinctly claim the subject matter which applicant regards as the invention."

1. Regarding claim 19

Concerning the above rejection the Examiner states:

> In claim 19, line 28, "additionally forming a third and fourth via pattern" renders the claim indefinite. It is not clear how a third and fourth via patterns are formed and are located.

Applicant has amended claim 19 by providing the limitation that the third and fourth via patterns are formed by etching the first and second etch patterns respectively through third dielectric layer material that is deposited in first and second via patterns respectively that are formed in the second dielectric layer. Support for this amendment can for example be found in the specification at page 11, lines 14-28 and page 13, lines 1-7. Applicant believes that the above described amendment overcomes the rejection and that currently amended claim 19 is therefore in a condition for allowance under 35 USC §112, second paragraph.

2. Regarding claims 23-30

Claims 23-30 depend from claim 19. As reasoned above, applicant believes that currently amended claim 19 is in a condition for allowance under 35 USC §112, second paragraph, applicant therefore believes that claims 23-30 are in a condition for allowance under 35 USC §112, second paragraph.

II. Claim rejections under 35 USC §102(e)

A. The Examiner rejected claims 5, 9 and 11 "under 35 USC §102(e) as being anticipated by Inohara et al. [US 5,976,972]."

1. Regarding claim 5

Applicant has amended claim 5 by reciting the additional limitation that the first dielectric layer is deposited "directly" on an interconnect line that is included in the substrate such that the first dielectric layer "contacts" the interconnect line. Support for this amendment can for example be found in the specification at page 13, lines 1-20 and in Figs. 6A and 6B. Inohara et al. Figs. 28 and 38 disclose structures employing a cap layer 54 that is interposed between wiring element 42 and layer 43, wherein layer 43 corresponds to applicant's first dielectric layer. Inohara et al. do not teach or disclose forming a trench through a dielectric layer such as applicant's second dielectric layer without also forming a via hole through a cap layer, such as Inohara et al. cap layer 54. Additionally, the Inohara et al. process for fabricating structures without a cap layer, such as the process and structures described and illustrated in col. 12, lines 30-48 and Figs. 26, 27, employ a trench that is fabricated on etch stop layer 44, which corresponds to applicant's second dielectric layer. By contrast, applicant's trench is formed through the third and second dielectric layers, see clause j. For the above reasons, applicant believes that claim 5 as currently amended is not anticipated by Inohara et al., US 5,976,972 and that amended claim 5 is in a condition for allowance under 35 USC §102(e).

3. Regarding claims 9 and 11

Claims 9 and 11 have been amended, making claims 9 and 11 dependent from claim 5. Applicant believes that currently amended claim 5 is in a condition for allowance under 35 USC §102(e) as reasoned above. Applicant therefore believes that claims 9 and 11 are in a condition for allowance under 35 USC §102(e).

Additionally regarding claim 9. Applicant has amended claim 9 to limit the mask layer to "combinations of photoresist mask layers and hard mask layers." Support for this amendment can for example be found in claim 9 as originally submitted. Inohara et al. teach photolithography (col. 13, line 21) and resist film 56 (col. 14, lines 50-56) but Inohara et al. do not disclose "combinations of photoresist mask layers and hard mask layers." Applicant therefore believes that claim 9 as currently amended is not anticipated by Inohara et al. and that amended claim 9 is in a condition for allowance under 35 USC §102(e).

Additionally regarding claim 11. The via hole that is filled with a conductive material extends through the first dielectric layer, while the Inohara et al. via hole extends additionally through a cap layer 54. Applicant therefore believes that claim 11 as currently amended is not anticipated by Inohara et al. and that amended claim 11 is in a condition for allowance under 35 USC §102(e).

B. The Examiner rejected claims 19, 23 and 28-30 "under 35 USC §102(e) as being anticipated by Lin [US 6,093,632]."

1. Regarding claim 19

Applicant respectfully submits that the Examiner has designated Lin layers 3 and 4 as both being "a first dielectric layer" as shown in the following statements in the Detailed Action.

- "a first dielectric layer (3, fig 4, col 5 lines 10-28) on a substrate (1/2)", see Detailed Action item 3 (a) at p.7

- "etching the third via pattern through the first dielectric layer 4", see item 3(i) [2] at p.9
- "the first dielectric layer comprising silicon oxide 4", see item 3(b) at p.7
- the Examiner has denoted Lin 1/2, Fig. 4, as a substrate, see item 3(a), at p.7, while basing most of the rejection on a designation of Lin layer 4 as the first dielectric layer thus implying that the Lin substrate is formed by 1/2/3, Fig.4

Applicant respectfully submits that the rejection of claim 19 does not meet the requirement that "The pertinence of each reference, if not apparent, must be clearly explained . . . ", see C.F.R. §1.104(c) (2), since Lin layers 3 and 4 are both designated by the Examiner as the "first dielectric layer" and since it is not clear whether the Examiner considers the Lin substrate as 1/2 or 1/2/3. Applicant therefore believes that the examination of claim 19 has failed to make out a *prima facie* case for rejecting the patentability of claim 19 under 35 USC §102(e). Applicant thus believes that claim 19 is not anticipated by Lin US 6,093,632 and that claim 19 as currently amended is in a condition for allowance under 35 USC §102(e).

Additionally regarding claim 19. The Lin trenches are etched through Lin layer 13 (i.e. the top dielectric layer of the Lin dielectric stack) see Fig. 7. The Lin trenches are then etched through layer 10, see col. 6, lines 3-8 and Fig. 7. The Lin trenches are thus etched through two dielectric layers. By contrast, applicant's trenches are etched only through the top dielectric layer only, i.e. the third dielectric layer, see clauses (h) and (i). Applicant therefore believes that claim 19 as currently amended is not anticipated by Lin US 6,093,632 and that amended claim 19 is in a condition for allowance under 35 USC §102(e).

Furthermore regarding claim 19. Applicant has amended claim 19 including the limitations that the substrate includes first and second interconnect lines (see claim preamble), the first dielectric layer is deposited "directly" on the "first and second interconnect lines" (see clause (a)), the first and second via patterns overlay the first and second interconnect lines (see clause (c)) and the first and second via holes contact the

first and second interconnect lines respectively (see clause (i)). Support for this amendment can for example be found in the specification at page 17 line 16 through page 18 line 5 and Figs. 9A through 9H. Applicant thus forms a structure wherein applicant's first dielectric layer, i.e. the layer upon which the sacrificial etch segments are formed, contacts the substrate and contacts the first and second substrate interconnect lines. By contrast, Lin forms a structure wherein a layer 3 (see Figs. 6,7) is interposed between Lin's interconnect lines 2 and the dielectric layer 4 upon which the sacrificial etch segments 10b are formed. Applicant therefore believes that claim 19 as currently amended is not anticipated by Lin US 6,093,632 and is thus in a condition for allowance under 35 USC §102(e).

Additionally regarding claim 19. Applicant has provided a further limitation reciting that the width of the first and second trench pattern is narrower than the width of the first and second via pattern respectively. Support for this amendment can for example be found in the specification at page 17 line 6 through page 18, line 16, page 10 lines 20-29 and Figs. 9A-9G. By contrast, the Lin trench patterns are wider than the via patterns, see col 5 line 54 through col 6 line 3 and Figs. 6,7. Applicant therefore believes that currently amended claim 19 is not anticipated by Lin US 6,093,632 and that amended claim 19 is in a condition for allowance under 35 USC §102(e).

2. Regarding claims 23 and 28-30

Claims 23 and 28-30 depend from claim 19. Applicant believes that currently amended claim 19 is in a condition for allowance under 35 USC §102(e) over Lin as reasoned above. Applicant therefore believes that claim 23 and 28-30 are in a condition for allowance under 35 USC §102(e).

Additionally regarding claim 28. Applicant has amended claim 28 to limit the mask layer to "combinations of photoresist layers and hard mask layers." Support for this amendment can for example be found in claim 28 as originally submitted. Lin teaches photoresist masks, see col 5 lines 29-43, but Lin does not disclose "combinations of photoresist mask layers and hard mask layers." Applicant therefore believes that currently

amended claim 28 is not anticipated by Lin US 6,093,632 and that amended claim 28 is in a condition for allowance under 35 USC §102(e).

III. Claim rejections under 35 USC §103

A. The Examiner rejected claims 13 and 15-18 "under 35 USC §103(a) as being unpatentable over Lin [US 6,093,632] in view of Inohara et al. [US 5,976,972]".

1. Regarding claim 13

With regard to the formation of the recited first and second trenches, the Examiner makes reference to Lin, stating in part

> d) forming the first trench on the etch stop layer such that the first trench does not overlay the sacrificial etch segment and wherein the first trench has a width WT1 (see the left trench 15b that does not overlay the sacrificial etch segment in fig 7);
>
> e) forming a second trench having a width WT2 on the etch stop layer such that
>
> [1] the second trench does not overlay the sacrificial etch segment,
>
> [2] the sacrificial etch segment is positioned between the first and second trenches,
>
> [3] the distance between the first and second trenches exceeds WS (see the right trench 15b that does not overlay the sacrificial etch segment wherein the distance between the left and right trenches 15b exceeding the sacrificial etch pattern's width in fig. 7); (see Detailed Action item No. 4, p.11,12)

Applicant respectfully submits that Lin's first and second trenches are formed through Lin etch stop layer 10, i.e. the layer which is provided with Lin's sacrificial etch pattern as well as the Lin patterns for the first and second vias, see col. 6 lines 3-8 and Fig. 7. By contrast, applicant's first and second trenches are formed on the etch stop layer (see clauses (d) (e) and (g)), i.e. the layer which is provided with applicant's via patterns as well as the sacrificial etch pattern. For the above reasons, applicant respectfully disagrees with the following Examiner's conclusion.

> With respect to claim 13, Lin, figs 4-8 and col 1-6, substantially discloses the claimed method of forming a structure on a substrate comprising the steips of: (see Detailed Action 4 at page 11)

For the reasons stated above, applicant believes that Lin provides an inappropriate basis for the rejection of claim 13 over Lin in view of Inohara et al. Applicant therefore believes that claim 13 is patentable over Lin in view of Inohara et al. and that claim 13 is in a condition for allowance under 35 USC §103(a).

Additionally regarding claim 13. The Examiner suggests to modify the process of Lin by employing trench widths that are narrower than the widths of the respective via patterns as taught by Inohara et al. (see Detailed Action at p.13). However, applicant notes that the Lin trench extends through the etch stop layer that includes the via patterns and the sacrificial etch pattern, (see above) while applicant's trench is formed on the etch stop layer. Applicant therefore respectfully submits that the wider via pattern of Inohara et al., if it could be combined with structure of Lin, would not result in a process as recited by applicant. Applicant therefore believes that claim 13 is patentable over Lin US 6,093,632 in view of Inohara et al. US 5,976,972 and that claim 13 is thus in a condition for allowance under 35 USC §103(a).

2. Regarding claims 15-18

Claims 15-18 depend from claim 13. Applicant believes that claim 13 is in a condition for allowance under 35 USC §103(a), as reasoned above. Applicant therefore believes that claims 15-18 are patentable over Lin in view of Inohara et al. and are in a condition for allowance under 35 USC §103(a).

B. The Examiner rejected claims 6, 7-8 and 10

> under 35 USC §103(a) as being unpatentable over Inohara et al [US 5,976,972] as applied to claim 1 above, in further view of Applied Materials Inc., "Applied Materials Announces Breakthrough low K dielectric film for High-Speed Cooper [sic] Chips", Business Wire, 10/6/1998, pp 1072 and Zhao et al. "A Cu/Low-k Dual Damascene Interconnect for High Performance and Low Cost Integrated Circuits", VLSl Technology 1998, Digest of Technical Paper 1998 Symposium, pp 28-29.

Claims 6, 7-8 and 10 have been amended to depend from amended claim 5. Applicant believes that amended claim 5 is patentable over the prior art of record, see Remarks at Section II A1. Applicant therefore believes that amended claims 6, 7-8 and 10 are patentable over the prior art of record and that amended claims 6, 7-8 and 10 are thus in a condition for allowance under 35 USC §103(a).

C. The Examiner rejected claims 24-27

> under 35 U.S.C. 103(a) as being unpatentable over Lin [US 6,093,632] as applied to claim 19 above, and in further view of Applied Materials Inc., "Applied Materials Announces Breakthrough low K dielectric film for High-speed Cooper [sic] Chips", Business Wire, 10/6/1998, pp 1072 and Zhao et al, "A Cu.Low-k Dual Damascene Interconnect for High Performance and Low Cost Integrated Circuits", VLSl Technology 1998, Digest of Technical Paper 1998 Symposium, pp 28-29.

Claims 24-27 depend from amended claim 19. Applicant believes that amended claim 19 is patentable over the prior art of record, see Remarks at Section II B1. Applicant therefore believes that claim 24-27 are patentable over the prior art of record and that claims 24-27 are thus in a condition for allowance under 35 USC §103(a).

Current Status Of The Claims

Claims 5-7 (currently amended)

Claim 8 (original)

Claims 9-11 (currently amended)

Claim 13 (previously amended)

Claim 15 (previously amended)

Claims 16-18 (original)

Claim 19 (currently amended)

Claim 23 (original)

Claim 24 (previously amended)

Claims 25-27 (original)

Claim 28 (currently amended)

Claim 29 (previously amended)

Claim 30 (original)

Condition Of Claims Remaining

In view of the above, applicant submits the claims remaining in the application are in a condition for allowance. The Examiner is invited to call the undersigned in the event the Examiner believes there are any issues remaining.

Respectfully submitted,

Dated: August 29, 2003

By: 

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